means for transmitting to the debug circuit a program counter value indicating the program counter of the processor.

Please cancel claim 21 without prejudice or disclaimer.

23. (Amended) A method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit, the method comprising steps of:

transmitting to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor.

Please cancel claim 32 without prejudice or disclaimer.

REMARKS

In response to the Office Action mailed April 18, 2002, Applicant respectfully requests reconsideration. To further the prosecution of this application, amendments have been made in the claims. The claims as now presented are believed to be in allowable condition.

Claims 1-33 were previously pending in this application. Claims 1, 3-5, 7, 12 and 23 have been amended. Claims 10, 21, and 32 have been cancelled. After this Amendment, claims 1-9, 11-20 and 22-31 and 33 remain pending for examination. Of these remaining claims, claims 1, 12, and 23 are independent.

Claim Objections

Claims 3-5 and 7 were objected to for various informalities. In response, Applicant has amended claims 3-5 and 7 in accordance with the suggestions provided by the Examiner. These amendments are for clarification only and are not intended to narrow the scope of the claims. It is believed that the claims are now clear, and therefore the objection of claims 3-5 and 7 should be withdrawn.

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Claim Rejections Under 35 U.S.C. §102

Claims 1-3, 5, 12-14, 16, 23-25, and 27 were rejected under 35 U.S.C. §102(b) as being anticipated by Razban (U.S. Patent No. 5,289,587, hereinafter "Razban"). In response, Applicant has amended the independent claims and submits the following remarks.

Razban is directed to a method for providing a microprocessor's program counter value external to a device on a dedicated bus so that an external in-circuit emulator system can generate a list of executed instruction addresses (col. 1, lines 17-21). In-circuit emulators (or ICE systems, as are known in the art) are a combination of external software and hardware used to design and troubleshoot software programs executing on a target microprocessor or controller. Razban provides a virtual program counter value to an external ICE system via a dedicated external bus 30 (col. 4, lines 35-41, col. 4, lines 66 through col. 5, line 4).

Independent claim 1 recites a microcomputer comprising at least one processor, a debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit, a system bus coupling the processor and debug circuit, and a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a program counter value indicating the program counter of the processor.

Razban does not anticipate that which is recited in claim 1. More particularly, Razban does not disclose a microcomputer comprising "at least one processor" and "a debug circuit" that are "implemented on a same integrated circuit," as recited. Razban teaches an external emulator system that has access to a program counter through a dedicated bus. Razban does not teach a processor and a debug circuit implemented on a same integrated circuit. Razban discloses an emulator which is located outside of the target processor. Therefore, Razban does not disclose the microcomputer as recited in claim 1. Claims 2-9 and 11 depend from claim 1 and are allowable for at least the same reasons.

Independent claim 12 recites a microcomputer comprising at least one processor, a debug circuit, a system bus coupling the processor in debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit, and means for transmitting to the debug circuit a program counter value indicating the program counter of the processor.

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Razban does not anticipate that which is recited in independent claim 12. As discussed above with reference to claim 1, Razban does not disclose a microcomputer comprising at least one processor and a debug circuit implemented on a same integrated circuit. Razban teaches an external emulator that accesses a program counter value of a microprocessor through a dedicated bus. Therefore, Razban does not anticipate that which is recited in claim 12, and the rejection should be withdrawn. Claims 13-20 and 22 depend from claim 12 and are allowable for at least the same reasons.

Independent claim 23 recites a method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit, the method comprising steps of transmitting, to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor.

Razban does not anticipate that which is recited in claim 23. In particular, Razban does not disclose an act of "transmitting, to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor" wherein the processor and debug circuit are "implemented on a same integrated circuit" as recited in claim 23. Razban teaches an emulator located separate from and outside of the target hardware. Razban does not teach transmitting a program counter value to a debug circuit on a communication link coupling the processor and the debug circuit, the processor and debug circuit being implemented on the same integrated circuit. Therefore, Razban does not anticipate that which is recited in claim 23, and the rejection should be withdrawn. Claims 24-33 depend from claim 23 and are allowable for at least the same reasons.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the number listed below.

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If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, please charge it to deposit account No. 23/2825.

Respectfully submitted,

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AMENDED CLAIMS SHOWING CHANGES

1. (Amended) A microcomputer comprising:

at least one processor;

a debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the processor and debug circuit; and

a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a program counter value indicating the program counter of the processor.

3. (Amended) The microcomputer according to claim 2, wherein the processor is further configured to transmit to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

4. (Amended) The microcomputer according to claim 3, wherein the processor is further configured to transmit to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

5. (Amended) The microcomputer according to claim 1, wherein the processor is further configured to transmit to the debug circuit a value indicating an increment of the program counter of the processor.

7. (Amended) The microcomputer according to claim 1, wherein the processor is further configured to transmit to the debug circuit [an] a signal indicating that a current process identifier value differs from a [processor] process identifier value of a previously-executed instruction.

12. (Amended) A microcomputer comprising:

at [lease] least one processor;

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a debug circuit, wherein the processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the processor and debug circuit; and

means for transmitting to the debug circuit a program counter value indicating the program counter of the processor.

23. (Amended) A method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit, the method comprising steps of:

transmitting, to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor.

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